

BRCM24C04SC

SOP-8

4 Kbit

I²C

1.7V

2.5~5.5V

1Mhz

1.7~2.5V

400Khz

CMOS

400uA

1.6mA

16

128

5ms

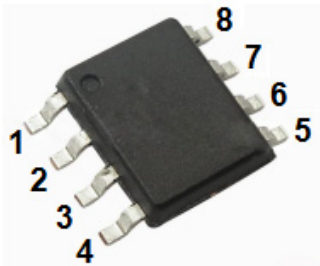
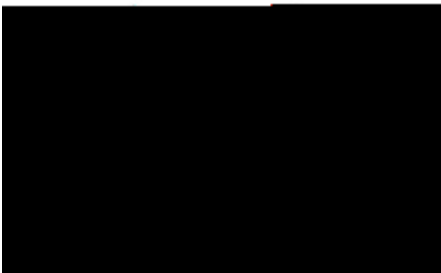
100

100

ESD HBM

6KV

+/-200mA;

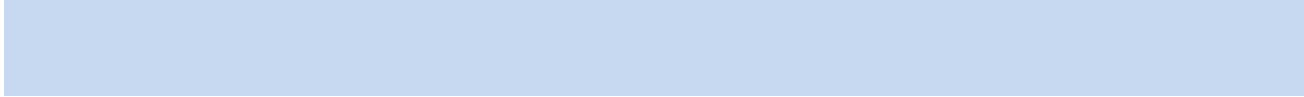


Pin	Name	Type	Description
1	NC	-	
2	E1	Input	
3	E2	Input	
4	GND	Ground	
5	SDA	I/O	/
6	SCL	Input	
7	WCB	Input	
8	VCC	Power	

			mA
			V

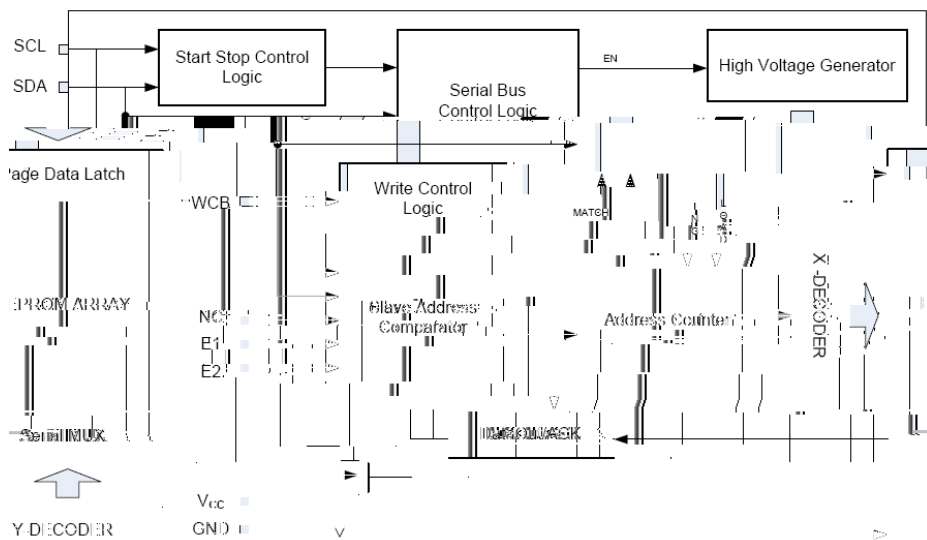
		Ñ				

[illegible][illegible]



		≤			≤			

≤



(1) SCL

Figure 1 Data Validity

SDA

SDA

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Figure 2 Start and Stop Definition

“ 0 ”

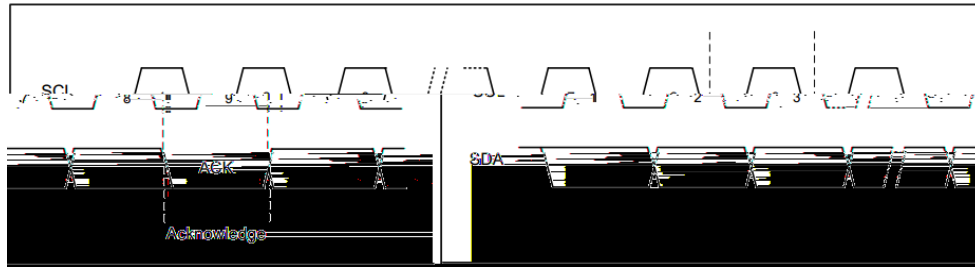


Figure 3 Output Acknowledge

H

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:(a)

,(b)

E2E1

0

4

1

8

/

E2E1

0

H

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WCB

Vcc

H

BRCM24C04SC

8

" 0 "

8

8

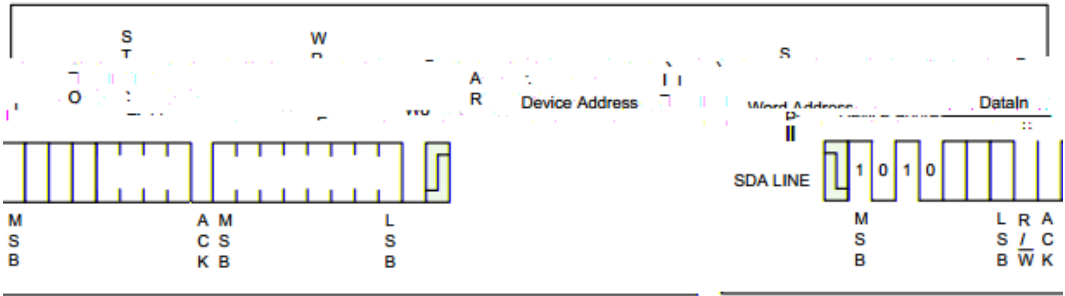
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" 0 "

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BRCM24C04SC

(5)

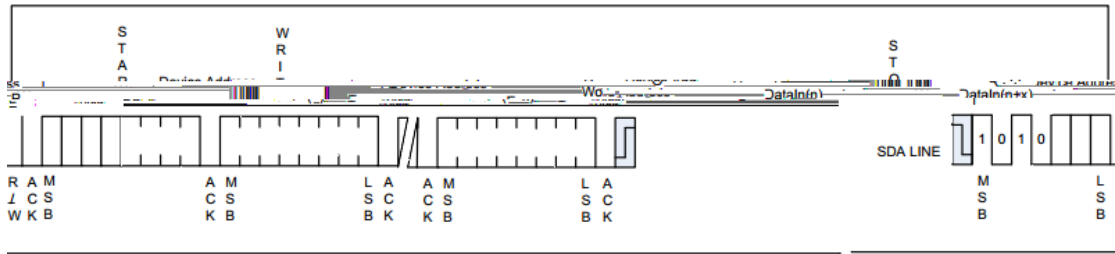


H

BRCM24C04SC

" 0 "

BRCM24C04SC



H

BRCM24C04SC

“ 0 ”

/

BRCM24C04SC

H

16

(a)1011b

(b)A5 / A401A7 / A6“ 00 ”

(c)A3 / A0

NoACK

H

ID

Lock ID

(a)1011b;

(b)A61;

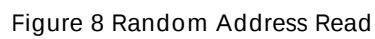
(c)xxxx xx1xx01

“ 1 ”

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7

8



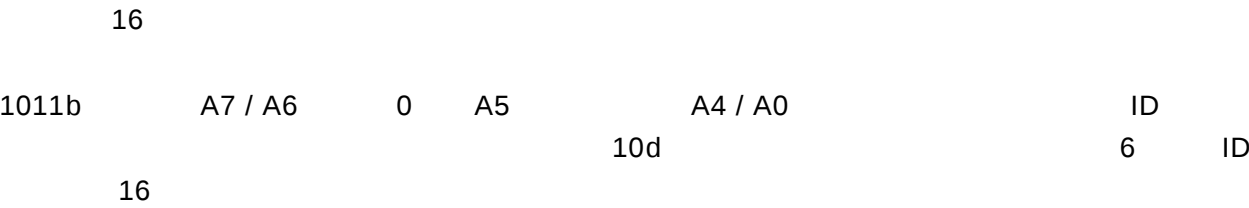
“ 0 ”

The diagram illustrates the I2C protocol timing. The SDA line (Serial Data) and SCL line (Serial Clock) are shown. The sequence of operations is as follows:

- Start (S):** Indicated by a high-to-low transition on the SDA line.
- Device Address (1010):** The first seven bits of the address are shown on the SDA line.
- Write (W):** Indicated by a high-to-low transition on the SCL line.
- Word Address (L R A M A):** The word address is shown on the SDA line.
- Read (R):** Indicated by a high-to-low transition on the SCL line.
- Stop (P):** Indicated by a low-to-high transition on the SDA line.
- Dummy Write:** A sequence of operations following the stop, including a start, device address, write, word address, and read.
- DataOut(n), DataOut(n+1), DataOut(n+x):** Data transfer operations are shown on the SDA line.
- End (E):** Indicated by a high-to-low transition on the SCL line.

Figure 9

H



H

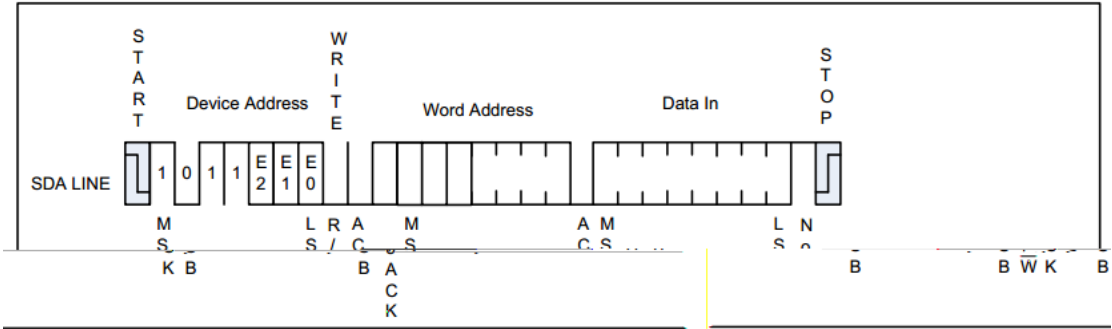
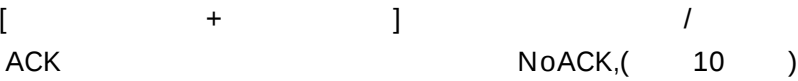
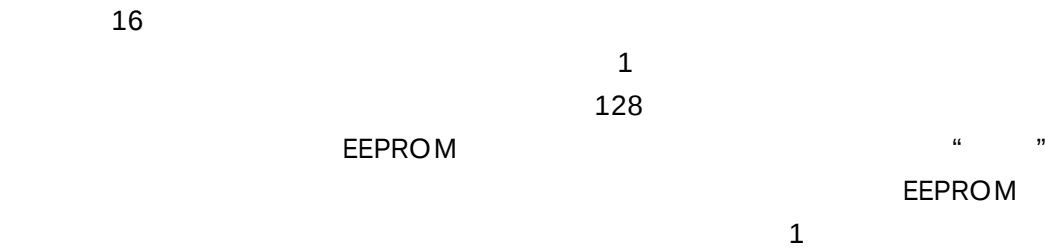


Figure 10 Lock Status Read (When Identification page locked, return NoACK after one data byte)

H



A7 A6 “ 10 ” 2 “ 10 ”
 80h
 128 16
 128 ACK
 7

□

□

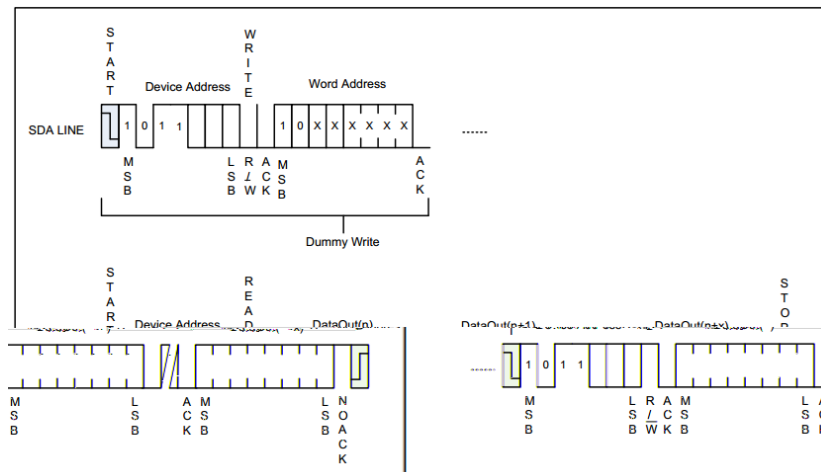
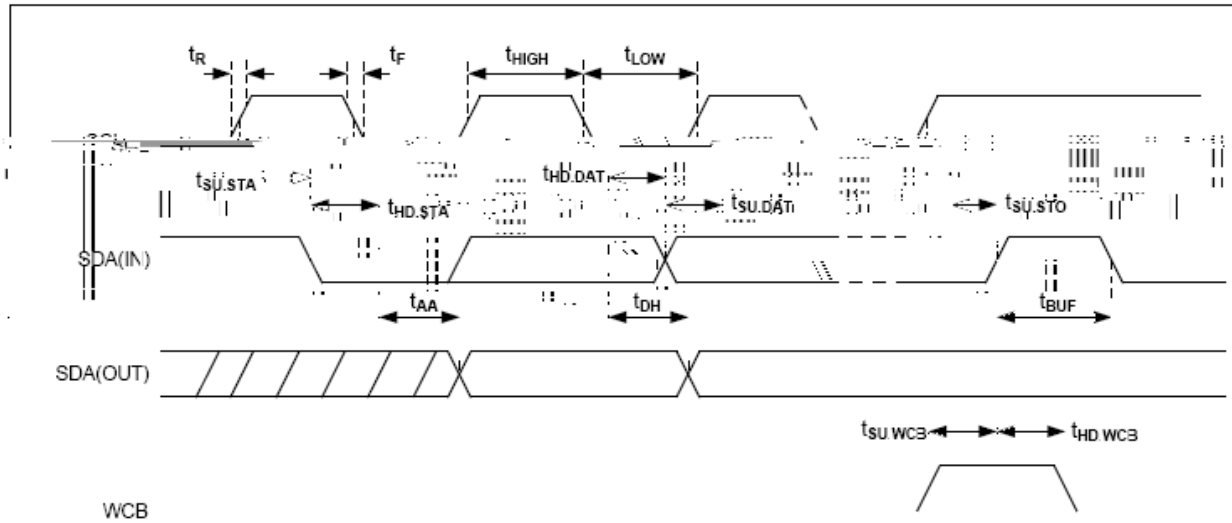
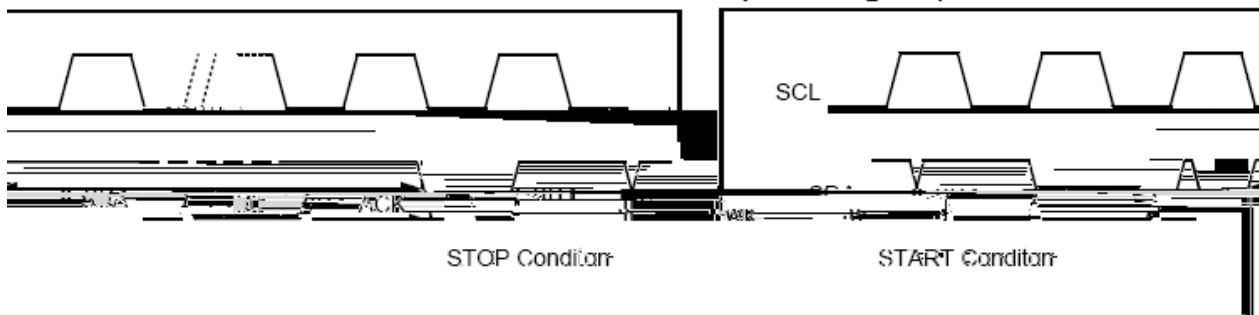


Figure 11 Sequential Read

Bus Timing

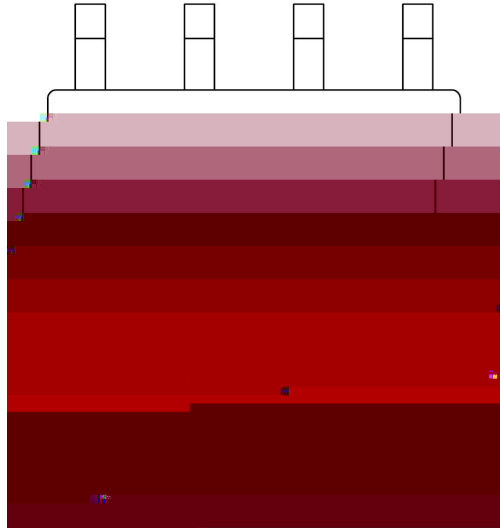


Write Cycle Timing

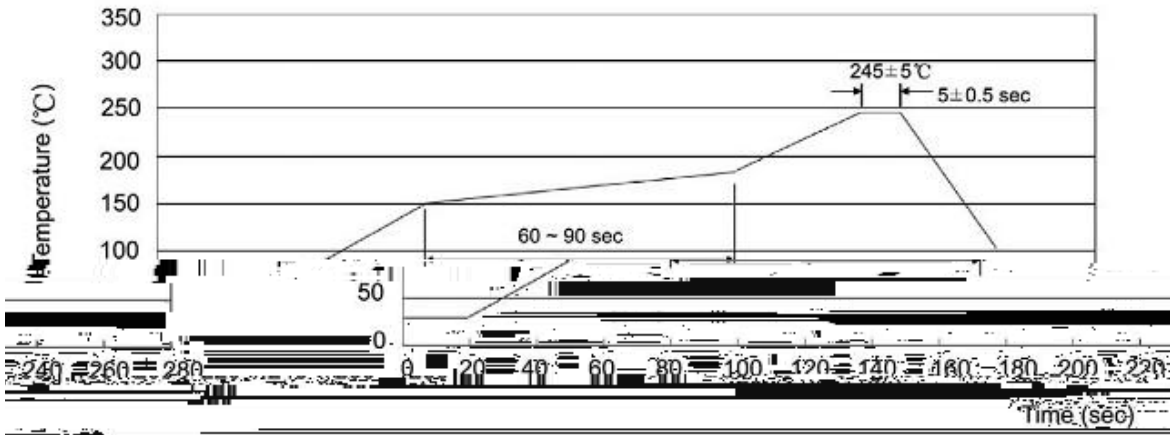


Note: The write-cycle time t_{W1} is the time from valid stop condition of a write sequence to the end of the initial clear/write cycle.





24C04



± ± ± ±

± ± ± ±

封装形式	包装数量					包装尺寸		
	只 卷盘	卷盘 盒	只 盒	盒 箱	只 箱		盒	箱